L3’s MFT1000 provides two complete PCM bit synchronizers, PCM decommutators and PCM simulators in a compact, portable package

L3 Telemetry & RF Products’ (L3 T&RF) MFT1000 is a network-attached IEEE-802.3at Ethernet multi-function telemetry unit providing a complete PCM telemetry system for one or two data streams.

IEEE-802.3at is a Power over Ethernet (PoE+) enabled network interface designed to eliminate the need for separate power cabling to network-attached devices.

The MFT1000 is a sister product to the PCIe Multi-Function Telemetry (MFT800) module. The MFT1000 provides two complete PCM bit synchronizers, PCM decommutators and PCM simulators in a compact, portable package.

PCM data processed by the MFT1000 is accurately synchronized with time using integrated IRIG time code reader, generator and translator functions.

The MFT1000 is ideally suited for quick-look applications, flight line checkout systems and portable configurations. A rich, robust and proven set of embedded functions typically off loads the host processor and can be applied to a wide variety of data communications solutions.

Both bit synchronizers provide 1 bps tuning resolution and support input rates to 40 Mbps with user programmable matched filtering. The user also has the ability to independently program the symbol timing, tracking range, automatic gain and DC tracking loop bandwidths to optimize the link performance for their specific application.

Both decoms support input interfaces from external I/O, the bit syncs or the simulators at 30 Mbps rates for 4-bit words and 40 Mbps rates for 8-bit words. Decom data outputs can be merged and transferred over the Ethernet output at aggregate rates up to 50 Mbps in TCP mode. The simulators provide high-resolution frequency programming and low jitter output for two independent PCM outputs at rates to 40 Mbps.

IRIG time synchronization and generation are supported via proprietary embedded digital processing that optimally acquires and tracks IRIG time signals and rejects noise. IRIG time functions are closely coupled with decommutation, providing high-accuracy time tagging of input data with 1-microsecond resolution for both real-time or playback applications.

**FEATURES/BENEFITS**

- Dual bit sync, decom, simulator functions
- L3 Vista™ software-compatible
- Power over Ethernet enabled
- Two PCM streams in one portable or rack-mountable unit (approximately 5.25 x 1.7 x 8 inches)
- CVSD voice support with digital filtering
- Ease of physical portability, fits in small spaces
- Extract clock/data from noisy PCM data streams at rates up to 40 Mbps
- Decodes, translates or generates IRIG-A, -B or -G time
- Time-tag PCM input frames with 1-microsecond resolution synchronized to an external source or on-board TCXO
- Status tag PCM input frames, including sync state, bit slip and CRC error detection
- Extract two asynchronous embedded frames, or fully decommutate a primary and an embedded stream
- Simulates telemetry data and formats up to 40 Mbps
- Viterbi decoder supporting 1/3, 1/2, 2/3, 3/4, 4/5, 5/6, 6/7, 7/8 rates
- 1-microsecond resolution for both real-time or playback applications
### MFT1000 Multi-Function Telemetry Unit

#### Specifications

**Bit Synchronizer (X2)**
- **Signal Range**: 50 mV to 5 Vpp (Auto Range) standard
- **Codes**: NRZ-L, NRZ-M, NRZ-S, BiØ-L, BiØ-M, BiØ-S, RZ, randomized NRZ-L (11, 15, 17)
- **Bit Rate**: 100 bps to 40 Mbps/20 Mbps (NRZ/Biphase Codes)
- **Tuning Resolution**: 1 bps
- **Loop Bandwidth**: 0.1% to 1.6% (percent of transition rate)
- **Bit Rate Tracking Range**: Bit rate <25 Mbps 0.1% to 5% of bit rate, Bit rate > 25 Mbps 0.1% to 4% of bit rate
- **AGC Loop Bandwidth**: 0.01% to 0.05% of bit rate
- **DC Tracking Loop Bandwidth**: 0.01% to 0.05% of bit rate
- **Outputs**: Clock/data with programmable phase/polarity
- **Output Drive/Termination**: TTL compatible CMOS: ±32 mA typical 33 Ω series termination, RS-422: 4 Vpp typical no load, 3 Vpp 120 Ω load
- **Viterbi decoders**: Standard for each channel, Rate = 1/3, 1/2, 2/3, 3/4, 4/5, 5/6, 6/7, 7/8 K = 7
- **Impedance**: 10 KΩ or 75 Ω programmable

**Input Channels Decommutators (X2)**
- **Input Termination**: CMOS: Hi-impedance, RS-422: 120 Ω load
- **Data Rates**: > 30 Mbps with 4 bpw > 40 Mbps with 8 bpw average, 50 Mbps aggregate
- **Input Code**: NRZ-L or randomized NRZ-L
- **Data Polarity**: Normal/Inverted/Auto
- **Data Alignment**: MSB/LSB first per stream
- **Input Levels**: TTL (data/clock) or RS-422 (data/clock)
- **Clock Input Phase**: 0° or 180° or Auto
- **Clock Duty Cycle**: 50 ±15%

**Data Buffer**
- **PCM Data Pass Qualifier**: Frame and subframe check or lock and per-word programmable in sorted or tag/data modes
- **Data Buffers**: Two independent 256-kword double buffers
- **Format**: Telemetry, status and time words sorted per application setup, tag-data or pass-through
- **Buffer Access Method**: Bus-mastering DMA controllers or slave reads and interrupts

**Other Inputs**
- **Data Pass Qualifier**: Frame and subframe Check or Lock and per word
- **Embedded Data Streams**: 2 maximum
- **Status to Host**: Frame sync state, subframe sync state, frame search detector, subframe search detector, bit slip detector, CRC error detector, interrupt state, interrupt overrun, active buffer size, bit rate
- **CVSD to DAC**: 2CH uses embedded data streams

**Frame and Subframe (Sorted Mode or Tag-Data) Characteristics**
- **Sync Pattern**: 64-bit max
- **Subframe Sync Method**: SFID, unique sync code, URC, FCC or none
- **Search-to-Lock**: 1 to 4 valid sync words
- **Lock-to-Search**: 1 to 4 invalid sync words
- **Error Threshold**: 0 to 3-bit
- **Sync Aperture**: ±0 or ±1-bit
- **CRC Size**: 4 to 65,536 telemetry words
- **CRC Error Checking**: Programmable polynomial and word location to 16th order

**Time-Tagging (Sorted Mode)**
- **Time Source**: Internal time clock optionally synchronized to external IRIG
- **Format**: BCD — µs to hundreds of days
- **Trigger Source**: End of minor frames
- **Resolution**: 1 µs

**Statutagging (Sorted Mode)**
- **Trigger Source**: End of minor frames

**Output Channels (Simulators) (X2): Modes of Operation**
- **Packed data**: A single data buffer is bit-packed at setup and continuously transmitted
- **Streaming**: Alternates between two data buffers under real-time host control
- **Burst**: Transmits 1–2 buffers of data and stops
- **Instruction**: Instructions and data are written at setup. Instructions specify the bpw, repeat count and jump command allowing the sequence to repeat

**Data Buffer**
- **Packed Data**: 4 Mb x 16 bits shared, programmable buffer sizes for each simulator
- **Streaming**: 4 Mb x 16 bits shared, programmable buffer sizes for each simulator
- **Burst**: 4 Mb x 16 bits shared, programmable buffer sizes for each simulator
- **Instruction**: 2 Mb instruction/data pairs shared

**Outputs**
- **Data Rates**: 10 bps to 40 Mbps
- **Data Rate Resolution**: 1 bps
- **Synthesizer Accuracy**: ±0.5 ppm
- **Time-Based Accuracy**: Initial error ±2 ppm, temperature stability ±0.25 ppm, total error ±0.6 ppm over 20 yrs.
- **PCM Data Codes**: NRZ-L, NRZ-M, NRZ-S, BiØ-L, BiØ-M, BiØ-S, RZ, randomized NRZ-L (11, 15, 17)
- **Outputs**: Clock/data with programmable phase/polarity
- **Output Drive/Termination**: CMOS: ±32 mA typical 33 Ω series termination, RS-422: 4 Vpp typical no load, 3 Vpp 120 Ω load
- **Clock Output Phase**: 0° or 180°
- **Clock Source**: Internal/external
- **Viterbi Encoder Rates**: 1/3, 1/2, 2/3, 3/4, 4/5, 5/6, 6/7, 7/8 K=7

* Requires future software update
**SPECIFICATIONS**

**TIME CODE READER/GENERATOR/TRANSLATOR:**
**INPUTS (APPLIES TO READER MODE ONLY)**

| Format                  | Digital: PWM  
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Analog: IRIG-A, -B or -G forward</td>
</tr>
</tbody>
</table>

| Playback Rates          | A&B: 1/4, 1/2, 1, 2, 4, 8, 16  
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>G: 1/4, 1/2, 1, 2, 4, 8</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Carrier Frequency Range</th>
<th>±5% of nominal</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mark Amplitude</td>
<td>200 mV to 10 V (auto-range)</td>
</tr>
<tr>
<td>Impedance</td>
<td>10 kΩ or 75 Ω programmable</td>
</tr>
<tr>
<td>Modulation Ratio</td>
<td>2:1 to 6:1</td>
</tr>
<tr>
<td>Error detection</td>
<td>Error frame bypass option</td>
</tr>
<tr>
<td>Phase-Locked Loop</td>
<td>Tracks IRIG input time and generates time on signal loss</td>
</tr>
</tbody>
</table>

**INTERNAL TIME CLOCK**

<table>
<thead>
<tr>
<th>Modes of Operation</th>
<th>Translate or generate forward</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>1 μs</td>
</tr>
<tr>
<td>Time-Based Accuracy</td>
<td>Initial error ±2 ppm, temperature stability ±0.25 ppm, total error ±4.6 ppm over 20 yrs. TCXO</td>
</tr>
</tbody>
</table>

**OUTPUTS**

<table>
<thead>
<tr>
<th>Format</th>
<th>Analog: IRIG-A, -B or -G Digital PWM with CMOS or RS-422 driver</th>
</tr>
</thead>
<tbody>
<tr>
<td>Amplitude/Source</td>
<td>1 to 10 Vpp no load, 75 Ω standard I/O source impedance</td>
</tr>
<tr>
<td>Modulation Ratio</td>
<td>3:1 nominal</td>
</tr>
</tbody>
</table>

**FRONT PANEL INTERFACES**

| System LED Status       | Online, active, fault |
| IRIG LED Status         | Input present, time lock, master mode |
| Bit Sync LED Status (2) | Input signal present, phase lock, Viterbi lock |
| Decom/Sim LED Status (2)| Minor & major frame lock, check & verify Simulator active |

**REAR PANEL INTERFACES**

| MFT Interfaces          | DB-62 (female) |
| Network Interface       | RJ-45 jack, IEEE-802.3at 10/100 BaseT interface PoE+ powered device |
| Auxiliary DC Input      | 2.0 mm power jack, 12 VDC power adapter input |

**POWER**

| IEEE-802.3at            | Class 4 powered device, <25 W typical |
| +12 V Aux Input Supply  | Approx. 1.5 A typ., ±5%, not including output loading |

**NETWORK PERFORMANCE**

| TCP                     | Up to 50 Mbps aggregate data traffic, 16-bit common word size in a [controlled] network. Smaller common word sizes increase the network overhead lowering the data throughput when the TCP traffic starts increasing above the 80 to 85 Mbps range. |
| Chapter 10 Output       | Supported in Vista™ |

**ORDERING INFORMATION**

| MFT1000                  | Networked Multi-Function Telemetry Unit |

| CABLE ASSEMBLY/PANEL OPTIONS |

(Note: I/O connector and pinout compatible with the MFT800)

<table>
<thead>
<tr>
<th>Single-Ended Cable</th>
<th>2 bit sync inputs, IRIG input, IRIG out, 8 programmable CMOS I/O</th>
</tr>
</thead>
<tbody>
<tr>
<td>CBL-MFT800-SE</td>
<td></td>
</tr>
<tr>
<td>Auxiliary DC Input</td>
<td>2 bit sync inputs, IRIG input, IRIG out, 8 programmable RS-422 I/O</td>
</tr>
<tr>
<td>CBL-MFT800-DIF</td>
<td></td>
</tr>
<tr>
<td>MFT I/O Interface Panel PNL-MFT900</td>
<td>Table top or rack mount I/O panel with 10 triaxial and 20 BNC connectors for the following signals: 2 bit sync inputs (differential optional), IRIG input, 2 programmable analog outputs (e.g. IRIG out or simulator), 15 programmable CMOS I/O, 10 programmable RS-422 I/O</td>
</tr>
</tbody>
</table>

**SOFTWARE SUPPORT**

- Support with L3 Vista™ (version 4.6 or later).
  Please refer to the L3 Vista data sheet for more.

Telemetry & RF Products
VISTA CH10-SUP— VISTA CHAPTER 10 SUPPORT

L3 T&RF now offers the capability to record & playback (archive) data in IRIG 106 Ch. 10 format through their flight test application, Vista™. This capability enables the user to record and play back PCM/time data in IRIG 106 Ch. 10 format and is compatible with L3 T&RF’s MFT1000 Networked Multi-Function Telemetry Unit.

The MFT1000 provides the capability to decode PCM streams up to 40 Mbps and transmit Chapter 10 Time and PCM packets to the network. Recording and playback of Chapter 10 data can be performed using the Vista Chapter 10 Software Recorder/Player application.

Data Types Archived in Chapter 10 Format:
- PCM Packet Unpacked (16-Bit Alignment Mode)
- PCM Packet Packed (16-Bit Alignment Mode)
- PCM Packet Throughput (16-Bit Alignment Mode)