L3’s MFT800 is a PCI Express® compliant module providing a complete PCM telemetry system for 1 or 2 data streams.

The MFT800 is the successor to the previous generation PCI Multifunction Telemetry (MFT733A-PCI) module.

The MFT800 provides better than double the throughput performance in a module approximately 1/2 the size of the MFT733A-PCI.

The MFT800 provides two complete PCM bit synchronizers, PCM decommutators and PCM simulators in one short form factor PCIe module. PCM data processed by the MFT800 is accurately synchronized with time using integrated IRIG time code reader, generator and translator functions.

The MFT800 is ideally suited for quick look applications, flight-line checkout systems and portable configurations. A rich, robust and proven set of embedded functions typically off-load the host processor and can be applied to a wide variety of data communications solutions.

Both bit synchronizers provide 1 bps tuning resolution and support input rates to 30 Mbps with user programmable matched filtering. The user also has the ability to independently program the symbol timing, tracking range, automatic gain and DC tracking loop bandwidths to optimize the link performance for their specific application.

Both deoms support input interfaces from external I/O, the bit syncs or the simulators at 30 Mbps rates for 4-bit words and 40 Mbps rates for 8-bit words or larger. The simulators provide high-resolution frequency programming and low jitter output for two independent PCM outputs at rates to 40 Mbps.

IRIG time synchronization and generation are supported via proprietary embedded digital processing that optimally acquires and tracks IRIG time signals and rejects noise. IRIG time functions are closely coupled with decommutation, providing high-accuracy time tagging of input data with 1 microsecond resolution for both real-time or playback applications.

**FEATURES/BENEFITS**

- Dual bit synchronizers, decommutators and simulators
- Bus-mastering DMA channels support both input and output channels
- Extract clock and data from noisy PCM data streams at rates to 30 Mbps
- Decode, translate or generate IRIG-A, -B or -G time
- Time tag PCM input frames with 1 microsecond resolution synchronized to an external source or on-board TCXO
- Status tag PCM input frames, including sync state, bit slip and CRC error detection
- Extract two asynchronous embedded frames, or fully decommutate a primary and an embedded stream
- Simulate telemetry data and formats to 40 Mbps
- Viterbi decoder supporting 1/2 rates
- Numerous I/O for simultaneous support to external equipment (i.e. decryptors)
**MFT 800**
**PCIe Multi-Function Telemetry Module**

**SPECIFICATIONS**

**BIT SYNCHRONIZER (X2)**

- **Signal range**: 50 mV to 5 Vpp (Auto Range) standard
- **Codes**: NRZ-L, NRZ-M, NRZ-S, BiØ-L, BiØ-M, BiØ-S, randomized NRZ-L (11, 15, 17)
- **Bit rate (NRZ/Biphase Codes)**: 100 bps to 30 Mbps/15 Mbps
- **Tuning resolution**: 1 bps
- **Loop Bandwidth**: 0.1% to 1.6% (percent of transition rate)
- **Bit rate tracking range**: Bit rate <25 Mbps 0.1% to 5% of bit rate, Bit rate > 25 Mbps 0.1% to 4% of bit rate
- **AGC loop bandwidth**: 0.01% to 0.05% of Bit rate
- **DC tracking loop bandwidth**: 0.01% to 0.05% of Bit rate
- **Outputs**: Clock/data with programmable phase/polarity
- **Output drive/termination**: TTL Compatible CMOS; +/-32 mA typical, 33 Ω series termination
- **Viterbi decoders**: Standard for each channel, Rate = 1/2, K = 7 (Contact factory for other options)
- **Impedance**: 10 KΩ or 75 Ω Programmable

**INPUT CHANNELS DECOMMUTATORS (X2)**

- **Input termination**: CMOS:Hi-impedance RS-422: 120 Ω load
- **Data rates**: > 30 Mbps with 4 bps > 40 Mbps with 8 bps average
- **Input code**: NRZ-L
- **Data polarity**: Normal/Inverted/Auto
- **Data alignment**: MSB/LSB first per stream
- **Input levels**: TTL (data/clock) or RS-422 (data/clock)
- **Clock input phase**: 0 ° or 180 °
- **Clock duty cycle**: 50 ±15%

**DATA BUFFER**

- **PCM data pass qualifier**: Frame and subframe Check or Lock
- **Data buffers**: Two independent 64-kword double buffers
- **Format**: Telemetry, status and time words sorted per application setup, or pass-through
- **Buffer access method**: Bus-mastering DMA controllers or slave reads and interrupts

**OTHER INPUTS**

- **Data Pass Qualifier**: Frame and subframe Check or Lock and per word
- **Embedded Data Streams**: 2 maximum
- **Status to Host**: Frame sync state, subframe sync state, frame search detector, subframe search detector, bit slip detector, CRC error detector, interrupt state, interrupt overrun, active buffer size, bit rate

**FRAME AND SUBFRAME (SORTED MODE OR TAG-DATA) CHARACTERISTICS**

- **Sync Pattern**: 64-bit max
- **Subframe Sync Method**: SFID, unique sync code, URC, FCC or none
- **Search-to-Lock**: 1 to 4 valid sync words
- **Lock-to-Search**: 1 to 4 invalid sync words
- **Error Threshold**: 0 to 3-bit
- **Sync Aperture**: ±0 or ±1-bit
- **Frame Size**: 4 to 65,536 telemetry words
- **CRC Error Checking**: Programmable polynomial and word location to 16th order

**TIME-TAGGING (SORTED MODE)**

- **Time Source**: Internal time clock optionally synchronized to external IRIG
- **Format**: BCD — µs to hundreds of days
- **Trigger Source**: End of minor frames
- **Resolution**: 1 µs

**STATU-TAGGING (SORTED MODE)**

- **Trigger Source**: End of minor frames

**OUTPUT CHANNELS (SIMULATORS) (X2)**

**MODES OF OPERATION**

- **Packed data**: A single data buffer is bit packed at setup and continuously transmitted
- **Streaming**: Alternates between two data buffers under real-time host control
- **Burst**: Transmits one or two buffers of data and stops
- **Instruction**: Instructions and data are written at setup. Instructions specify the bwp, repeat count and jump command allowing the sequence to repeat

**DATA BUFFER**

- **Packed data**: 8 Meg x 16-bits shared, programmable buffer sizes for each simulator
- **Streaming**: 8 Meg x 16-bits shared, programmable buffer sizes for each simulator
- **Burst**: 8 Meg x 16-bits shared, programmable buffer sizes for each simulator
- **Instruction**: 4 Meg instruction/data pairs shared

**OUTPUTS**

- **Data rates**: 10 bps to 40 Mbps
- **Data rate resolution**: 1 bps
- **Synthesizer accuracy**: ±0.5 ppm
- **Time Base accuracy**: Initial Error ±2 ppm, Temperature Stability ±0.25 ppm, Total Error ±4.6 ppm over 20 years
- **PCM data codes**: NRZ-L, NRZ-M, NRZ-S, BiØ-L, BiØ-M, BiØ-S, randomized NRZ-L (11, 15, 17)
- **Outputs**: Clock/Data with programmable phase/polarity
- **Output drive/termination**: CMOS: ±32 mA typical, 33 Ω series termination RS-422: 4 Vpp typical no load, 3 Vpp 120 Ω load
- **Clock output phase**: 0 ° or 180 °
- **Clock source**: Internal/external
## SPECIFICATIONS CONTINUED

**TIME CODE READER/ GENERATOR/ TRANSLATOR INPUTS (APPLIES TO READER MODE ONLY)**

<table>
<thead>
<tr>
<th>Format</th>
<th>Analog: IRIG-A, -B or -G forward</th>
</tr>
</thead>
<tbody>
<tr>
<td>Playback rates</td>
<td>1/16, 1/8, 1/4, 1/2, 1, 2, 4, 8 or 16 times real-time</td>
</tr>
<tr>
<td>Carrier frequency range</td>
<td>±5% of nominal in a wide loop bandwidth mode</td>
</tr>
<tr>
<td>Mark amplitude</td>
<td>200 mV to 10 V (auto-range)</td>
</tr>
<tr>
<td>Impedance</td>
<td>1 MΩ or 75 Ω programmable</td>
</tr>
<tr>
<td>Modulation ratio</td>
<td>2:1 to 6:1</td>
</tr>
<tr>
<td>Error detection</td>
<td>Error frame bypass option</td>
</tr>
<tr>
<td>Phase-locked-loop</td>
<td>Tracks IRIG input time and generates time on signal loss; wide or narrow loop bandwidth (prog)</td>
</tr>
</tbody>
</table>

**INTERNAL TIME CLOCK**

<table>
<thead>
<tr>
<th>Modes of operation</th>
<th>Translate or generate forward</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>1 µs</td>
</tr>
<tr>
<td>Time Based accuracy</td>
<td>Initial Error Initial Error ±2 ppm, Temperature Stability ±0.25 ppm Total Error ±4.6 ppm over 20 years TCXO</td>
</tr>
</tbody>
</table>

**OUTPUTS**

<table>
<thead>
<tr>
<th>Format</th>
<th>Analog: IRIG-A, -B or -G Digital PWM with CMOS or RS-422 driver</th>
</tr>
</thead>
<tbody>
<tr>
<td>Amplitude/Source</td>
<td>1 to 10 Vpp no load, 75 Ω standard termination I/O source impedance</td>
</tr>
<tr>
<td>Modulation ratio</td>
<td>3:1 nominal</td>
</tr>
</tbody>
</table>

**CONNECTORS AND CABLE ASSEMBLY OPTIONS**

- **Rear panel**: DB-62 (female)
- **Single-Ended cable**: 2-bit sync inputs, IRIG Input, IRIG Out, 8 programmable CMOS I/O
- **Differential cable**: 2-bit sync inputs, IRIG Input, IRIG Out, 8 programmable RS-422 I/O
- **MFT I/O interface option**: Table top or rack mount I/O panel with 10 triaxial and 20 BNC connectors for the following signals: 2-bit sync inputs (Differential optional) IRIG Input 2 programmable analog outputs (e.g. IRIG Out or Simulator) 15 programmable CMOS I/O 10 programmable RS-422 I/O

**CARD TYPE**

- **PCI Express**: Short Form Factor, X4 connector per PCIe CEM spec, 1 lane used

**POWER**

<table>
<thead>
<tr>
<th>Voltage</th>
<th>2 A typical ±5%</th>
</tr>
</thead>
<tbody>
<tr>
<td>+3.3 V supply</td>
<td>500 mA typical ±5%, Not including output loading</td>
</tr>
</tbody>
</table>

**ENVIRONMENTAL**

**OPERATING ENVIRONMENT**

<table>
<thead>
<tr>
<th>Temperature</th>
<th>0 °C to 55 °C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Humidity</td>
<td>up to 90% non-condensing</td>
</tr>
<tr>
<td>Altitude</td>
<td>up to 10,000 feet</td>
</tr>
</tbody>
</table>

**STORAGE ENVIRONMENT**

<table>
<thead>
<tr>
<th>Temperature</th>
<th>-40 °C to 85 °C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Humidity</td>
<td>up to 95% non-condensing</td>
</tr>
<tr>
<td>Altitude</td>
<td>not tested or specified</td>
</tr>
</tbody>
</table>

## ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MFT800</td>
<td>PCIe Multi-Function Telemetry Module (Note: I/O cables ordered separately)</td>
</tr>
</tbody>
</table>

### CABLE ASSEMBLY/PANEL OPTIONS

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CBL-MFT800-SE</td>
<td>Single ended signal breakout cable assembly (12 signals)</td>
</tr>
<tr>
<td>CBL-MFT800-DIF</td>
<td>Differential signal breakout cable assembly (12 signals)</td>
</tr>
<tr>
<td>PNL-MFT800</td>
<td>Rack mount or table top signal I/O panel single ended (15) and differential (10) signals, analog I/O (5)</td>
</tr>
</tbody>
</table>

### SOFTWARE SUPPORT

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CBL-MFT800-SE</td>
<td>Single ended signal breakout cable assembly (12 signals)</td>
</tr>
<tr>
<td>CBL-MFT800-DIF</td>
<td>Differential signal breakout cable assembly (12 signals)</td>
</tr>
<tr>
<td>PNL-MFT800</td>
<td>Rack mount or table top signal I/O panel single ended (15) and differential (10) signals, analog I/O (5)</td>
</tr>
</tbody>
</table>
This presentation consists of L3 Technologies, Inc. general capabilities information that does not contain controlled technical data as defined within the International Traffic in Arms (ITAR) Part 120.10 or Export Administration Regulations (EAR) Part 734.7-11 Data, including specifications, contained within this document are summary in nature and subject to change at any time without notice at L3’s discretion. Call for latest revision. All brand names and product names referenced are trademarks, registered trademarks, or trade names of their respective holders.