L-3 Interstate Electronics Corporation (IEC) Antares™ NTDS I/O boards provide a direct interface between military computers and the industry standard VMEbus. These high performance boards offer many features that make them easy to install, easy to program and easy to operate.

**HIGH PERFORMANCE NTDS**

*Bit-slice technology provides on-board intelligence.*

Where high speed, specialized NTDS sequence control is required, L-3 IEC’s Antares NTDS bit-slice design is the proven solution. The bit-slice architecture is tailored for intelligent NTDS I/O protocol control. Users can construct I/O instruction sequences that execute rapidly without requiring host processor intervention. Users can access Antares NTDS’ 15 versatile instructions to transfer and manipulate I/O data, test and set host processor semaphores, and service VMEbus interrupts in response to I/O events.

On-board intelligence allows users to carry out complex NTDS protocols without assistance from the host processors. Up to 19 Antares NTDS boards can easily operate in a single VME chassis with a single processor or multiple processors.

**Full DMA operation of both NTDS data transfers and I/O instruction execution.**

System designers must account for various minimum and maximum NTDS sequence latency requirements, as well as accommodate NTDS DMA transfer speeds. Some military equipment, particularly peripheral devices such as single data converters, display consoles and communication links, have specialized timing requirements that can burden host processors or slower NTDS I/O boards. Antares NTDS I/O boards allow users to transfer data on all four NTDS I/O paths (Input (IB), Output (OB), External Function (EF) and External Interrupt (EI)) at the same time. To meet the full duplex demands of modern MIL-STD-1397 interfaces, a parallel NTDS I/O board must have the ability to transfer DMA External Function (EF) data while the Output Data (OD) DMA transfer is active. Antares products are the only VME boards that can activate and transfer an EF word on an inter-computer channel (Category II) while an OD transfer is also active.
EASY TO PROGRAM

The software interface is functionally similar to the AN/UYK-43 military computer. I/O chains written for the AN/UYK-43, -7, -44, or -20 can be easily ported to execute on the Antares NTDS board, providing a path to transition legacy systems to modern, open systems.

Antares NTDS boards execute sequences of instructions directly from VMEbus memory. The on-board program counters (total of five) are used to access memory, read an instruction and execute it. The command program counter is "loaded" by the CPU via a single 32-bit "store" to the VMEN10 board. At that point, the Antares NTDS board begins to execute its instructions directly from memory, without any further CPU intervention. The I/O chains will normally have been generated at compile time within the user program with common data structures, records or arrays. The address supplied to the board command program counter is a pointer to the start of the I/O chain to be executed. All I/O operations are controllable from a high-order language.

MIL-STD-1397 VERSATILITY

Antares NTDS boards provide a comprehensive range of compatible interface types on the VMEbus, including standard parallel and serial NTDS types, as well as special interfaces. The open architecture of the VMEbus provides an excellent path for migrating legacy systems hosted in military equipment to high performance microcomputer systems.

ANTARES NTDS 4002

The Antares 4002 I/O main board has on-board shared memory as well as internal registers, offering system designers expanded flexibility. The on-board memory allows the user to store I/O instruction chains in the board's shared memory to provide increased instruction execution speed without accessing the VMEbus. This feature provides the capability to execute sophisticated I/O chains where response times are critical. Software selectable memory offsets provide automatic adjustments for addresses of I/O chains and data buffers stored anywhere within 1MB boundaries on the VMEbus, including the VMEN10 on-board memory.

The internal registers of the Antares 4002 allow users to do "on-the-fly" processing of 1B, 0B, EF and EI data in parallel (e.g., "running" 32-bit ones complement checksum on both input and output messages simultaneously).

User Control

The Antares NTDS 4002 is programmable and operates similarly to the Navy's AN/UYK-43 computer I/O controller. The board can execute instructions out of any VMEbus memory. The instructions may be generated in a high level language such as Ada or C and are normally placed in memory at system load time. The VMEbus host processor initiates VMEN10 operations with a single 32-bit store of the starting address of the first instruction in memory to be executed. No further host processor intervention is required. The I/O board continues to read and execute instructions from memory until an "end of chain" indication is encountered.

The Antares 4002 provides 1 Mbyte of on-board general purpose shared static memory, which may be mapped anywhere in the 32-bit (or 24-bit) address space of the VMEbus on 1MB boundaries and provides a nominal 200 nanosecond access time. Memory is accessed automatically by the 4002's processor when the board's programmed VMEbus address matches the mapped address. No VMEbus cycles are used by the 4002 processor when accessing on-board memory, allowing I/O instructions to reside on the board, while reducing VMEbus cycles and speeding up execution times.
Applications Flexibility

Entire NTDS I/O software protocols can be processed by the Antares 4002 without the intervention of a host computer. The instruction sequences are easy to design and write, and host CPU time dedicated to the I/O functions is minimal. The Antares 4002’s parallel processing greatly enhances the throughput of I/O transactions; not just the data rate on the cable, but also the sequencing and verification processes of the software protocol.

The Antares 4002 can sustain the full MIL-STD-1397 data rates of types A, B and E while interfacing with external equipment. L-3 IEC also offers a 4002 long-cable Type B Antares 4002 type B board to support extra long cable applications.

The Antares 4002 supports full duplex operation to allow transmitting External Function words while an Output Buffer is active during operations in inter-computer mode (Category II). The capability to send or receive forced External Function words (those sent without the use of the External Function Request/External Interrupt Enable signal) is supported. The board allows users to send forced Output words and Input/EI IDAs for special test or operational conditions.

Programming

A powerful set of “on-the-fly” data processing codes are available to manipulate the incoming or outgoing data in real-time, at no expense to the host processor and very little overhead to the transfers. NTDS inter-computer software protocols typically require inconvenient instruction sequences for modern microprocessors. An example is calculating the checksum of 32-bit values using ones complement arithmetic. Performing the ones complement checksum is a simple process on the Antares 4002; the actual calculation adds only 400 nanoseconds per transfer, considerably less than the time required using the host computer’s instruction set. This user-selectable on-the-fly process allows the software to respond with positive or negative acknowledgements to an incoming message within 15 microseconds of the completion of a buffer transfer, including verifying a checksum on all of the buffer data.
ANTARES NTDS I/O BOARDS

ANTARES NTDS 4002-E BOARD


Full Duplex Operations

Four DMA channels provide independent data transfer for Input/Output Buffers and External Interrupt/Function Buffers simultaneously without tying up CPU resources. Each DMA channel is associated with a separate ALU register for quick access and simultaneous operations such as calculating checksums.

CPU Overhead is Minimized

Full board control of the interface protocol for automatic processing of checksums is provided. Handshaking (sis/sos), Error Processing (timing, illegal conditions, sink time-outs), and the generation of Interrupts (buffer complete, time-outs, errors). The Antares 4002/HPE is capable of initiating and performing data transfers automatically by following any user specified protocol.

Software Commands Similar to the UYK-43

Specified I/O protocols and requirements can be defined using a set of powerful high-level commands similar to those found in the UYK family of military computers. These instruction sequences, called I/O chains, may range from the most basic input/output protocols to extremely complex chains. I/O chains may be generated in a high-level language like Ada or C and can be stored in either VME or on-board SRAM memory, eliminating the need for custom PROM sets. 1 MByte of on-board SRAM is available with each Antares 4002/HPE board.

The VME base memory address can be set via a combination of front panel and board resident switches. A special memory address offset register allows for use of generic relocatable code in multiple boards.

High Performance

Throughput on the Antares 4002/HPE conforms to the limits specified in MIL-STD-1397C for the NTDS burst (300kw/sec) and non-burst (200kw/sec) mode. In addition, the Antares 4002/HPE supports VME burst mode at eight words for output and four words for input, providing more efficient use of the VMEbus bandwidth. All combinations of NTDS burst mode (thirty-two 32-bit word blocks), non-burst mode (one 32-bit word), non-parity and parity (33-bit transmission detects single bit errors) are supported and are software selectable.

On-board buffering isolates the NTDS input/output, allowing for performance at the optimum specification requirements independent of the level of VMEbus activity. Performance is therefore consistent and predictable over a wide range of conditions. Immediate transmission of External Functions and immediate reception of External Interrupts occurs without queuing and with minimal latency.

The on-board SRAM can be used to store user specified I/O chains, providing increased instruction execution speed without accessing user memory or the VMEbus. This allows for critical and predictable timing of I/O sequences. Additionally, a 32-bit 100KHz real-time clock provides 10-microsecond granularity and a range of 10 hours for close timing control.
ANTARES NTDS 4001 PRODUCT SPECIFICATIONS

32-bit 100 kHz Real-time Clock
The Antares NTDS 4001 includes a 32-bit clock value with 10 microsecond granularity for close timing control of I/O sequences for simulation and debug.

On-the-Fly Data Processing of I/O Data
Users may apply a data processing operation on each NTDS word transferred to or from the Antare 4001 board. The operations include: swap 16-bit integers in a 32-bit word; Logical AND, Logical OR or Logical XOR with a mask; and arithmetic operations. No additional memory references or host processor overhead are encountered when using data processing operations.

Antares NTDS 4001 Specifications

VMEBus:
- DTB Master A32/24:D32/16
- Requester R(0-3) RWD
- Bus Timer BTO (102 microseconds)
- DTB Slave A32/24/16:D32/16
- Interrupter I (1-7), R0AK
- Weight Under 2 lbs
- Size 6U, 160mm x 233mm, single slot
- Storage Temp. -25° to 85 °C
  90% relative humidity, non-condensing
- Operating Temp. 0° to 50 °C
  90% relative humidity, non-condensing
- Forced Air Cooling Required

NTDS:
- NTDS Types A, B, D and E are available.
- Word Size: 32 or 16-bit transfers for Types A, B
  32-bit transfers for Types D and E
- NTDS Mode: (A and B only)
  Category I, acting as a computer (CAT 1)
  Category I, acting as a peripheral (CAT 3)
  Category II (Intercomputer)

Power Consumption

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<th>+5V</th>
<th>+12V</th>
<th>-12V</th>
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<tr>
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<td>0</td>
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<tr>
<td>D</td>
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</tr>
<tr>
<td>E</td>
<td>.900 A</td>
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**ANTARES NTDS 4002 PRODUCT SPECIFICATIONS**

The Antares NTDS 4002 is easily installed and integrated into the user environment through switches/jumpers. The board operates automatically in both MASTER and SLAVE modes as required. VME Interrupt Request Levels and VMEbus Master Timeout are software selectable. Users may select, via a set of hardware switches, the following: a) privileged or non-privileged data access mode; b) 24 or 32-bit addressing; c) VME memory base address; and d) BUS REQUEST anc BUS GRANT levels.

**Antares NTDS 4002 Specifications**

- **DTB Master**: A32/24:D32, switch selectable
- **Requester**: R(0-3) RWD, switch selectable fairness mode
- **Bus Timer**: BTO (102/408/816/1224 microseconds)
- **DTB Slave**: A32/24/16:D32/16, switch selectable
- **Interrupter**: I (1-7), ROAK, software selectable
- **Weight**: Under 2 lbs
- **Size**: 6U, 160mm x 233mm, single slot
- **Humidity**: 0 to 95% non-condensing
- **Storage Temp.**: -25° to 85 °C
- **Operating Temp.**: 0° to 50 °C
- **Forced Air Cooling Required**

**Power Consumption**

<table>
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</tr>
<tr>
<td>E</td>
<td>900 mA</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

**SOFTWARE DRIVERS AVAILABLE**

- SunOS (series 3 and 4)
- AT&T UNIX
- HP-UX
- HP-RT
- IRIX

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Headquartered in New York City, L-3 Communications is a prime system contractor in aircraft modernization and maintenance, C3ISR (Command, Control, Communications, Intelligence, Surveillance and Reconnaissance) systems and government services. L-3 is also a leading provider of high technology products, systems and subsystems.

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